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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,906	11/14/2003	Jin K. Kim	H0004299 US	7661

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EXAMINER	
VAN ROY, TOD THOMAS	
ART UNIT	PAPER NUMBER
2828	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,906	KIM, JIN K.	
	Examiner	Art Unit	
	Tod T. Van Roy	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9,10,15-21,23-28,31,32 and 37-40* is/are rejected.

7)☒ Claim(s) *7-8,11-14,22,29-30,33-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims1-3, 5-6, 9-10, 15-18, 20-21, 23-25, 27-28, and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Tandon et al. (US 2004/0218655).

With respect to claim 1, Tandon discloses a vertical cavity surface emitting laser (VCSEL) (fig.3a) comprising: a substrate (fig.3a #120), a first mirror stack over the substrate (fig.3a #130), an active region having a plurality of quantum wells over the first mirror stack (fig.3a #112, [0041]), a tunnel junction over the active region (fig.3a #102), the tunnel junction including a modulation doped layer (fig.5a #304, can be incorporated into fig.3a [0065], considered to be a modulation layer based on the layers #330,332 being 5nm each, adding to 10nm total, within the defined limit as taught in the applicant's specification [0028]), and a second mirror stack over the tunnel junction (fig.3a #132).

With respect to claim 2, Tandon discloses the modulation layer is doped with a concentration greater than 1x10^19 ([0067]).

With respect to claim 3, Tandon discloses the modulation layer to include a first and second layer (fig.5a #330,332), the first layer being a highly dopable material or a dopant layer ([0067]).

With respect to claim 5, Tandon discloses a p-layer of the tunnel junction includes the modulation doped layer (fig.6a #406, can be incorporated into fig.3a [0070]).

With respect to claim 6, Tandon discloses the n-layer to be of a InGaAs compound (fig.6a #430).

With respect to claim 9, Tandon discloses an n-layer of the tunnel junction to include the modulation doped layer (fig.5a #304).

With respect to claim 10, Tandon discloses the p-layer to be of a GaAs compound (fig.5a #306).

With respect to claim 15, Tandon discloses an n-type spacer adjacent the active region (fig.3a #116), and wherein the first mirror stack is an n-type DBR ([0008], [0040]).

With respect to claim 16, Tandon discloses a p-type spacer adjacent the active region (fig.3a #118), and wherein the second mirror stack is an n-type DBR ([0008], [0040]).

Claim 17 is rejected for the descriptions given in the rejections to claims 15 and 16.

With respect to claim 18, Tandon discloses the p-layer is doped with carbon with a concentration greater than 1x10^19 ([0072]).

With respect to claim 20, Tandon discloses the first and second mirror stacks are upper and lower mirror stacks (fig.3a).

With respect to claim 21, Tandon discloses the modulation layer is used for both p-layer and n-layer of the tunnel junction (fig.6a).

With respect to claim 23, Tandon discloses a tunnel junction including a modulation doped layer (fig.5a #304, can be incorporated into fig.3a [0065], considered to be a modulation layer based on the layers #330,332 being 5nm each, adding to 10nm total, within the defined limit as taught in the applicant's specification [0028]).

With respect to claim 24, Tandon discloses the modulation layer is doped with an effective concentration greater than 1x10^19 ([0067] layer #330, [0062] layer #332 as taught in [0066], both layers have doping over 1x10^19 so effective doping requirement would be met).

With respect to claim 25, Tandon discloses the modulation layer to include a first and second layer (fig.5a #330,332), the first layer being a highly dopable material or a dopant layer ([0067]).

With respect to claim 27, Tandon discloses a p-layer of the tunnel junction includes the modulation doped layer (fig.6a #406, can be incorporated into fig.3a [0070]).

With respect to claim 28, Tandon discloses the n-layer to be of an InGaAs compound (fig.6a #430).

With respect to claim 31, Tandon discloses an n-layer of the tunnel junction to include the modulation doped layer (fig.5a #304).

With respect to claim 32, Tandon discloses the p-layer to be of a GaAs compound (fig.5a #306).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 4 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tandon in view of Gardner et al. (US 2005/0023549).

With respect to claims 4 and 26, Tandon teaches a VCSEL including a tunnel junction with modulation layer, but does not disclose the total thickness of the first layer and the second layers to be about .1-2nm. Gardner teaches a tunnel junction wherein the total thickness of the junction is taught to be 2nm, or the individual layers are taught to be 1nm ([0023]). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the modulation layers of Tandon with the thickness of

Gardner in order to bring about a low resistance and low series voltage drop when reverse biased (Gardner, [0023]).

Claim19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tandon in view of Bour et al. (US 2004/0161013).

With respect to claim 19, Tandon teaches the active region to be chosen for the desired wavelength ([0042]), but does not teach the material to be of InGaAsP or AlInGaAs. Bour teaches a long wavelength VCSEL with a tunnel junction using InGaAsP ([0010]). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the active region teaching of Tandon with the InGaAsP material of Bour in order to vary the wavelength based on the given application.

Claims 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour in view of Gardner.

With respect to claims 37 and 40, Bour teaches a long wavelength VCSEL ([0002]) comprising: an indium-based semiconductor alloy substrate ([0010]), a first mirror stack over the substrate (fig.1 #12), an active region having a plurality of quantum wells over the first mirror stack (fig.1 #15, [0009]), a tunnel junction over the active region (fig.1 #17, including an additional layer inside of the tunnel junction fig.2 #63, [0015]), and a second mirror stack over the tunnel junction (fig.1 #14). Bour does not teach the tunnel junction to have a modulation doped layer (layers #63,52 not taught to be thin enough to constitute a modulation layer from applicant's definition). Gardner

teaches a tunnel junction wherein the total thickness of the junction is taught to be 2nm, or the individual layers are taught to be 1nm ([0023]). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the modulation layers of Bour with the thickness of Gardner in order to bring about a low resistance and low series voltage drop when reverse biased (Gardner, [0023]).

With respect to claims 38 and 39, Bour and Gardner teach the tunnel junction VSCEL as outlined in the rejection to claim 37, and Bour additionally teaches the modulation layer to be of two layers (fig.2 #52,63) the first layer being highly doped with a concentration greater than 1x10^19 ([0014]).

Allowable Subject Matter

Claims 7-8, 11-14, 22, 29-30, and 33-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 7 is believed to be allowable based on the fact that a VCSEL containing a tunnel junction with a modulation doped layer of the AlInAs type, grown using p-type doped AlAs and InAs was not found to be taught in prior art.

Claim 8 is allowable as it depends from claim 7.

Claim 11 is believed to be allowable based on the fact that a VCSEL containing a tunnel junction with a modulation doped layer formed of SiAs and AlGaInAs was not found to be taught in the prior art.

Claims 12-14 are allowable as they depend from claim 11.

Claim 22 is allowable for the reasons given for the allowability of claims 7 and 11.

Claim 29 is believed to be allowable based on the fact that a tunnel junction with a modulation doped layer of the AlInAs type, grown using p-type doped AlAs and InAs was not found to be taught in prior art.

Claim 30 is allowable as it depends from claim 29.

Claim 33 is believed to be allowable based on the fact that a tunnel junction with a modulation doped layer formed of SiAs and AlGaInAs was not found to be taught in the prior art.

Claims 34-36 are allowable as they depend from claim 33.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tod T. Van Roy whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVR

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PRIMARY EXAMINER